

16798 U.S. PTO
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Anwar Ali  
Tauman T. Lau  
Max M. Yeung

Title: INTEGRATED CIRCUIT DESIGN FOR BOTH INPUT OUTPUT LIMITED AND CORE LIMITED INTEGRATED CIRCUITS

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Date of Deposit: July 3, 2003

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Pamela Gerik  
Pamela Gerik

(For new non-provisional applications under 37 CFR § 1.53(b))

Enclosed are the following items:

1. The Commissioner is hereby authorized to charge the filing fee to LSI Logic Corporation deposit account no. 12-2252/02-6109. **A duplicate of this page is enclosed.** The filing fee is calculated as shown below.

|                           |    |       |   |             |          |
|---------------------------|----|-------|---|-------------|----------|
| Total Claims              | 20 | -20 = | 0 | x \$18.00 = | \$0.00   |
| Independent Claims        | 3  | -3 =  | 0 | x \$84.00 = | \$0.00   |
| Multiple Dependent Claims |    |       |   | Fee:        |          |
| Basic Fee:                |    |       |   |             | \$750.00 |
| Total:                    |    |       |   |             | \$750.00 |

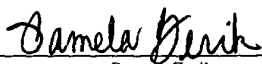
2. Request & Certification under 35 U.S.C. 122(b)(2)(B)(i).
3. Patent application which includes: 18 pg. specification; 4 pg. claims (1-20); 1 pg. abstract.
4. Formal drawings of Figs. 1-7 on 4 sheets.
5. Newly executed Declaration/Power of Attorney.
6. Newly executed Assignment w/cover sheet.
7. Return receipt postcard.

Respectfully submitted,

Kevin L. Daffer  
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Attorney for Applicants

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Date: July 3, 2003

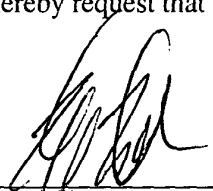
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|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|------------|-----------------------|------------------|--------|----------------------------------------------------------------------------------------------|
| <p align="center"><b>CERTIFICATE OF EXPRESS MAIL</b><br/><b>UNDER 37 C.F.R. §1.10</b></p> <p>"Express Mail" mailing label number: EV205758725US<br/>DATE OF DEPOSIT: July 3, 2003</p> <p>I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. §1.10 on the date indicated above and is addressed to:</p> <p align="center">Assistant Commissioner for Patents<br/>Box Patent Application<br/>Washington, DC 20231</p> <p align="center"><br/>Pamela Gerik</p> | <p align="center"><b>REQUEST AND CERTIFICATION</b><br/><b>UNDER</b><br/><b>35 U.S.C. 122(b)(2)(B)(i)</b></p> <table border="1"> <tr> <td data-bbox="748 338 1019 386">Atty Docket Number:</td> <td data-bbox="1019 338 1393 386">5201-26601</td> </tr> <tr> <td data-bbox="748 386 1019 434">First Named Inventor:</td> <td data-bbox="1019 386 1393 434">Anwar Ali et al.</td> </tr> <tr> <td data-bbox="748 434 841 653">Title:</td> <td data-bbox="841 434 1393 653">INTEGRATED CIRCUIT DESIGN FOR BOTH INPUT OUTPUT LIMITED AND CORE LIMITED INTEGRATED CIRCUITS</td> </tr> </table> | Atty Docket Number: | 5201-26601 | First Named Inventor: | Anwar Ali et al. | Title: | INTEGRATED CIRCUIT DESIGN FOR BOTH INPUT OUTPUT LIMITED AND CORE LIMITED INTEGRATED CIRCUITS |
| Atty Docket Number:                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 5201-26601                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                     |            |                       |                  |        |                                                                                              |
| First Named Inventor:                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Anwar Ali et al.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                     |            |                       |                  |        |                                                                                              |
| Title:                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | INTEGRATED CIRCUIT DESIGN FOR BOTH INPUT OUTPUT LIMITED AND CORE LIMITED INTEGRATED CIRCUITS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                     |            |                       |                  |        |                                                                                              |

I hereby certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing. I hereby request that the attached application not be published under 35 U.S.C. 122(b).

July 3, 2003

Date

  
Kevin L. Daffer, Reg. No. 34,146

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing**.

Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under 35 U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications eighteen months after filing, the applicant **must** notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign or international application. **Failure to do so will result in abandonment of this application (35 U.S.C. 122(b)(2)(B)(iii)).**

Burden Hour Statement: This collection of information is required by 37 CFR 1.213(a). The information is used by the public to request that an application not be published under 35 U.S.C. 122(b) (and the PTO to process that request). Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This form is estimated to take 6 minutes to complete. This time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.